LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
H0001996 (4960)	10/024030
APPLICANT	
Lopac, et al.	
FILING DATE	GROUP
December 18, 2001	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
IBP	AA	3,739,462	06/19/73	Method for Encapsulating Discrete Semiconductor Chips	29	577	01/06/71
IBP	BB	3,784,878	01/08/74	Matrix Assembly	317	101	07/06/72
IBP	CC	4,567,542	01/28/86	Multilayer Ceramic Substrate with Interlayered Capacitor	361	321	04/23/84
IBP	DD	4,800,459	01/24/89	Circuit Substrate Having Ceramic Multilayer Structure Containing Chip-Like Electronic Components	361	321	01/24/89
IBP	EE	4,994,938	02/19/91	Mounting of High Density Components on Substrate	361	401	12/28/88
IBP	FF	5,324,687	06/28/94	Method for Thinning of Integrated Circuit Chips for Lightweight Packaged Electronic Systems	437	225	10/16/92
IBP	GG	5,353,498	10/11/94	Method for Fabricating an Integrated Circuit Module	29	840	07/09/93
IBP	HH	5,422,513	06/06/95	Integrated Circuit Chip Placement in a High Density Interconnect Structure	257	668	10/04/93
IBP	II	5,495,394	02/27/96	Three Dimensional Die Packaging in Multi-Chip Modules	361	764	12/19/94
IBP	JJ	5,550,086	08/27/96	Ceramic Chip Form Semiconductor Diode Fabrication Method	437	209	12/27/95
IBP	KK	5,689,091	11/18/97	Multi-Layer Substrate Structure	174	255	09/19/96
IBP	LL	5,745,984	05/05/98	Method for Making an Electronic Module	29	834	07/10/95
IBP	MM	5,811,879	09/22/98	Stacked Leads-Over-Chip Multi-Chip Module	257	723	11/20/97
IBP	NN	5,939,782	08/17/99	Package Construction for Integrated Circuit Chip with Bypass Capacitor	257	698	03/03/98
IBP	OO	5,943,216	08/24/99	Apparatus for Providing a Two-Sided, Cavity, Inverted-Mounted Component Circuit Board	361	761	06/03/97
IBP	PP	6,038,133	03/14/00	Circuit Component Built-In Module and Method for Producing the Same	361	760	11/20/98
IBP	QQ	6,049,123	04/11/00	Ultra High Density Integrated Circuit Packages	257	686	09/22/97
IBP	RR	6,153,928	11/28/00	Substrate for Semiconductor Package, Fabrication Method Therof, and Stacked-Type Semiconductor Package Using the Substrate	257	686	05/16/97
IBP	SS	6,154,366	11/28/00	Structures and Processes for Fabricating Moisture Resistant Chip-on-Flex Packages	361	704	11/23/99
IBP	TT	6,180,881	01/30/01	Chip Stack and Method of Making Same	174	52.4	05/05/98

IBP	U	6,271,469	08/07/01	Direct Build-Up Layer on an Encapsulated Die Package	~~174~~	~~52.4~~	11/12/99
IBP	V	6,333,566	12/25/01	Semiconductor Having High Density Packaging Thereof	~~257~~	~~790~~	11/08/99

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	XX							

OTHER REFERENCES (*Including Author, Title, Date, Pertinent Pages, Etc.*)

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EXAMINER	DATE CONSIDERED
ISHWAR B. PATEL	11/27/02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.